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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/313,037	05/17/1999	LOUIS M. MELI	PHN-17.438	3381

24737 7590 10/06/2005

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
BAKER, PAUL A	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 10/06/2005

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/313,037
Filing Date: May 17, 1999
Appellant(s): MELI, LOUIS M.

Michael F. Hoffman

For Appellant

EXAMINER'S ANSWER

This is in response to the substitute appeal brief filed 29 July 2005.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

No evidence is relied upon by the examiner in the rejection of the claims under appeal.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1 – 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Palowski US Patent 5,426,769 in view of Dallas Semiconductor "DS87C550 Product Preview".

In regards to claim 1, Palowski discloses an instruction execution unit having an instruction set that contains a memory access instruction in table 3, execution of the memory access instruction causing the instruction execution unit to issue memory access signals with an access address determined from the currently selected address table 3 mov instructions producing signals in figure 10 states 2-4 on port 2; and

a control register that is instruction-settable in column 14 line 59 to respective control states that control whether or not the processing device updates the at least two addresses as a side-effect of executing the memory access instruction in the second table in column 15 (in comparison to first table).

Palowski does not disclose a register circuit for storing at least two addresses in parallel;

an address selector arranged to cycle a set of states in which respective ones of the at least two addresses become a currently selected address respectively;

or the execution of the memory access instruction further causing the address selector to cycle to a next one of the states.

Dallas Semiconductor discloses a register circuit for storing at least two addresses in parallel on page 14 1st column 3rd paragraph, DPTR0 and DPTR1,

an address selector (data pointer select bit SEL page 14 1st column 4th paragraph) arranged to cycle a set of states in which respective ones of the at least two addresses become a currently selected address respectively on page 15 1st paragraph,

and execution of the memory access instruction further causing the address selector to cycle to a next one of the states on page 15, 1st column 1st paragraph and 2nd table of assembly code.

Palowski discloses in column 5 line 62 through column 6 line 2 that reducing the number of clock cycles required for external data access is desirable and a stated goal of Palowski. Dallas Semiconductor states on page 14, 1st column 3rd paragraph that the incorporation of two data pointer registers improves the efficiency of data moves. This efficiency is accomplished by eliminating the need to continually having to load the single DPTR register of the native 8051 architecture with the source and destination addresses (Thereby reducing the number of clock cycles required for external data

access). This increases code density, and reduces the time required for each move operation. The combination of Palowski and Dallas, while modifying the same facet of the 8051 architecture, do so in such a way that the combination of the two does not alter the functionality of the other; therefore there is a reasonable expectation of success for the combination of the two prior art. Since Dallas Semiconductor states that the incorporation of two data pointer registers improves the efficiency of data moves, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate Dallas's shadow DPTR register in Palowski.

In regards to claim 2, Palowski further discloses each control state specifies respective update actions for all of the at least two addresses in column 14 lines 58 and 59.

In regards to claim 3, Palowski further discloses the control states specifying a choice of at least no-update, update by incrementing with a predetermined value and update by decrementing with the predetermined value in column 14 lines 61 – 65.

In regards to claim 4, Palowski further discloses that execution of the memory access instruction further causes the instruction execution unit to perform, upon the currently selected address, the update action that is specified by the control state of the control register for that one of the at least two addresses that is the currently selected address in column 15 lines 26 – 28.

In regards to claim 5, Palowski further discloses the instruction set includes a load from memory instruction and store to memory instruction, for causing the execution unit to respond ro the execution the memory access instruction in column 15 lines 22 – 25.

In regards to claim 6, Applicant discloses as prior art a program for executing alternately the load from memory instruction and the store to memory instruction, for an address addressed by a first one and a second one of the at least two addresses respectively on page 2 lines 6 and 7. Applicant does not disclose the setting the control register to one of the control states that causes both the first one and second one of the address to be updated. Palowski discloses the enable and disable for the auto-increment/auto-decrement may be set individually in column 14 lines 63-65. Since the combination of Palowski and Dallas would provide a system, that once set up, would provide source to destination data moves consisting of alternate "move source to register" and "move register to destination" instructions (with no ancillary instructions), it would have been obvious at the time of invention to one of ordinary skill in the art to set both auto-updates for the purpose of moving blocks of data from one memory region to another memory region.

In regards to claim 7, Applicant discloses as prior art a program for executing alternately the load from memory instruction and the store to memory instruction, for an

address addressed by a first one and a second one of the at least two addresses respectively on page 2 lines 6 and 7. Applicant does not disclose the setting the control register to one of the control states that causes only one of the first one and second one of the address to be updated. Palowski discloses the enable and disable for the auto-increment/auto-decrement may be set individually in column 14 lines 63-65. Since the combination of Palowski and Dallas would provide a system, that once set up, would provide source to destination data moves consisting of alternate "move source to register" and "move register to destination" instructions (with no ancillary instructions), it would have been obvious at the time of invention to one of ordinary skill in the art to set only one of the auto-updates for the purpose of transferring blocks of data to and from a memory mapped IO port.

In regards to claim 8, Dallas Semiconductor further discloses the address selector cycles back and forth between states that select a first and second one of at least two addresses respectively on page 14, 1st paragraph.

In regards to claim 9, Palowski further discloses each of four pages having an address and data SFR, given Dallas Semiconductor's motivation of improved efficiency of data moves given on page 14, 1st column 3rd paragraph; it would have been obvious at the time of invention to one of ordinary skill in the art to include additional address registers one for each extra address SFR in order to improve the efficiency of inter-page data transfers. By incorporation of Palowski within Dallas Semiconductor the user would

be able to cycle through selected states of the address SFR with the ability of incrementing or decrementing each address.

In regards to claim 10, Palowski discloses an instruction execution unit having an instruction set that contains a memory access instruction in table 3, execution of the memory access instruction causing the instruction execution unit to issue memory access signals with an access address determined from the currently selected address table 3 mov instructions producing signals in figure 10 states 2-4 on port 2; and

a control register in communication with said register selector register and said control register being instruction-settable in column 14 line 59 to respective control states that control whether or not the processing device updates the at least two addresses will be updated as a side-effect of executing the memory access instruction in the second table in column 15 (in comparison to first table).

Palowski does not disclose discloses a register circuit for storing at least two addresses in parallel;

an address selector including a register selector register and a logic circuit collectively arranged to cycle a set of states in which respective ones of the at least two addresses become a currently selected address respectively;

or the execution of the memory access instruction further causing the address selector to cycle to a next one of the states.

Dallas Semiconductor discloses a register circuit for storing at least two addresses in parallel in on page 14 1st column 3rd paragraph DPTR0 and DPTR1,

an address selector including a register selector register (data pointer select bit SEL page 14, 1st column 4th paragraph) and a logic circuit (inherent to perform cycling operation between the two address pointers) collectively arranged to cycle a set of states in which respective ones of the at least two addresses become a currently selected address respectively on page 14 1st paragraph,

and execution of the memory access instruction further causing the address selector to cycle to a next one of the states on page 14, 1st column 1st paragraph and 2nd table of assembly code.

Palowski discloses in column 5 line 62 through column 6 line 2 that reducing the number of clock cycles required for external data access is desirable and a stated goal of Palowski. Dallas Semiconductor states on page 14, 1st column 3rd paragraph that the incorporation of two data pointer registers improves the efficiency of data moves. This efficiency is accomplished by eliminating the need to continually having to load the single DPTR register of the native 8051 architecture with the source and destination addresses (Thereby reducing the number of clock cycles required for external data access). This increases code density, and reduces the time required for each move operation. The combination of Palowski and Dallas, while modifying the same facet of the 8051 architecture, do so in such a way that the combination of the two does not alter the functionality of the other; therefore there is a reasonable expectation of success for the combination of the two prior art. Since Dallas Semiconductor states that the

incorporation of two data pointer registers improves the efficiency of data moves, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate Dallas's shadow DPTR register in Palowski.

(10) Response to Argument

Applicant asserts Dallas does not disclose the limitation "a register circuit for storing at least two addresses in parallel". Applicant has specifically drawn issue with "circuit" and "parallel" and asserts that Dallas does not disclose a register circuit nor that the two addresses are parallel; stating Dallas' disclosure that "DPTR1 is located at the next two register locations (up from DPTR0)" is evidence of applicant's argument.

The examiner respectfully disagrees with applicant's assertions. The applicant's arguments rely upon a narrow interpretation of the limitations "parallel" and "circuit". The specification of the present application does not define either "parallel" or "circuit" in a manner that supports applicant's narrow interpretation. When the specification does not provide a specific definition of a limitation used within the claims the examiner must consider the broadest possible interpretation of the limitation when considering the patentability of said claim.

Applicant has provided no context within the specification of what is the applicant's intended meaning of the word "parallel". It is clear that the address registers are not loaded simultaneously since the disclosed invention does not support this

operation, so "parallel" is not describing the process of loading or accessing the registers simultaneously. "Parallel" within the context of VLSI design would indicate that the two registers are geographically located next to each other. Principles of VLSI design place two adjacent registers in a register file parallel to each other on the silicon. Dallas' disclosure that DPTR0 and DPTR1 are located in two adjacent locations within the register file indicates that the two registers are parallel on the silicon die. Furthermore, to the system programmer; both the DPTR0 and DPTR1 registers appear as the same register since DPTR is used to address both registers, as evidenced by the 2nd code sample on page 15 of Dallas. The system programmer viewing the DS87C550's method of operation would conclude that DPTR0 and DPTR1 are stored in parallel within the microcontroller regardless whether each register is discretely addressable or not. The examiner asserts that there are at least two interpretations of "parallel" in which Dallas does disclose this limitation and therefore anticipates the "parallel" limitation.

Dallas' DS87C550 disclosed in "DS87C550 EPROM High Speed Micro with A/D and PWM, Product Preview" is a generational improvement chip over the original Intel 8051 microcontroller, as such Dallas designed the DS87C550 to be backwards compatible with code written for the 8051. The original 8051 had a single data pointer register DPTR, which required the repeated loading of the source and destination addresses when moving blocks of data from one location to another. In order to increase the efficiency of moving blocks of data from one location to another, Dallas

incorporated a second data pointer register which alleviates the need to constantly reload the data pointer register when moving blocks of data, and named the two registers DPTR0 and DPTR1. DPTR0 is at the same register address as the DPTR in the 8051, in order to maintain backwards code compatibility, and the DPTR1 is located at the next two addresses following the DPTR0 registers. Disclosure of this arrangement is provided in the section "DUAL DATA POINTER WITH INC/DEC" first and second paragraphs. This arrangement of DPTR0 and DPTR1 is what the applicant is relying upon as evidence to their arguments. However, immediately following this, Dallas further explains that these two data pointer registers are treated as a singly mapped data pointer register through the use of a data pointer select bit SEL. When SEL=0, if the programmer uses the data pointer register DPTR, the data pointer register DPTR0 is used in the memory access instruction. Conversely, when SEL=1, if the programmer uses the data pointer register DPTR, the data pointer register DPTR1 is used in the memory access instruction. Dallas further provides another control bit, toggle select bit TSEL, whose effect when set to 1, automatically toggles the SEL bit after every use of the DPTR register. This has the effect of mapping both the DPTR0 and DPTR1 data pointer registers to the DPTR register, such that to a programmer these two distinct data pointer registers are stored in parallel. Therefore when considering the entire disclosure of Dallas' dual data pointer registers and not just the section relied upon by the applicant, one of ordinary skill in the art would conclude that Dallas anticipates applicant's claim limitation of "a register circuit for storing at least two registers in parallel". The ability for a programmer to individually address DPTR0 and

DPTR1 is an additional feature of the DS87C550 that is separate and distinct to the use of DPTR and does not teach away from the applicants claimed invention.

Dallas reads upon applicant's "register circuit". Dallas discloses on page 14 "The second data pointer, DPTR1 is located at the next two register locations (up from DPTR0), and is selected using the data pointer select bit SEL (DPS.0). If SEL=0 then DPTR0 is the active data pointer. Conversely, if SEL=1, then DPTR1 is the active data pointer" and "Another useful feature of the device is its ability to automatically switch the active data pointer after a DPTR-based instruction is executed". This indicates that these operations on the registers are beyond the capability of a standard register's operation and therefore circuitry to perform these operations is inherent to the DS87C550. For this reason Dallas anticipates applicant's "register circuit" limitation.

Applicant asserts that that there would be no reasonable expectation of success when combining the references, and that "Pawloski teaches an external decoder and memory space that includes a control special function register SFR that can be programmed to enable and disable auto-incrementing", and in order to provide the update of the internal registers of DPTR0 and DPTR1 taught by Dallas a structure would be required to permit access to the internal registers by Palowski's decoder.

The examiner respectfully disagrees with applicant's assertions. To arrive at applicant's understanding of the combination of Dallas and Pawloski, Dallas must be

bodily incorporated within Pawloski. The office relies upon the decision set forth in *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981), which states that bodily incorporation is not required for a proper rejection under 35 U.S.C. §103. The examiner was not relying on the bodily incorporation of the two references but incorporating the features taught by Dallas and used in the rejection of independent claims 1 and 10 within the invention disclosed by Pawloski. Incorporation of these two references in the manner relied upon by the examiner to reject claims 1 and 10 of the present application produces a system in which all elements are internal within the same structure. Therefore a system with a reasonable expectation of success exists when combining Pawloski and Dallas in the manner specified by the examiner.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Mano Padmanabhan 9/29/05

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